A REGISTER FILE WITH A SELECTABLE KEEPER CIRCUIT

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BACKGROUND OF THE INVENTION

Field of the Invention

[0001] This disclosure relates to memory, and, more particularly, to register file design.

Description of the related art.

[0002] In today's computer systems, there are various levels of storage devices. These various levels of storage support different needs. For example, one need in some computer systems is the need for mass storage that are relatively low priced. This need is frequently met by large, inexpensive fixed-disk storage devices. The tradeoff for these large, inexpensive fixed-disk storage devices is that these devices have slow access times.

[0003] In comparison, there is, at times in certain systems, a need for memory devices that can provide very quick access for the reading and/or writing of data. A type of such memory devices is referred to as register files, which are often on the same die as a processing unit that accesses them, as they are accessed very frequently. In addition to quick access times, preferably, these devices are robust, and consume low power.

[0004] FIG. 1 illustrates a read portion of a prior art dynamic register file design. In this example, eight data cells **140** are multiplexed to support a dynamic local bit line **110**. A clock signal **122** is used to precharge the dynamic local bit line **110** to a known value through transistor **124**. Keeper circuit **130** is utilized to "keep" the precharged value on the dynamic local bit line **110** during an evaluation

phase of a register file access. During the evaluation phase, for a set of eight data cells **140** possibly containing a data value to be "read", one of the read enable lines **142** may be used to enable the read of a corresponding data value **141**. Upon the assertion of a read enable line **142**, a corresponding stored data value may be driven on the local bit line **110**. If no read enable line **142** is enabled for the set of eight data cells **140**, the keeper circuit **130** is utilized to retain the precharged value on the local bit line **110**. The local bit lines are then utilized to drive a subsequent multiplexing circuit to form a global bit line (not shown).

[0005] Applicants have recognized a number of conflicting requirements for efficient and/or effective implementations of such dynamic designs, especially in a new generation of high operating frequency integrated circuits. For example, in order to minimize the evaluation time and thus increase the operating frequency, it is desirable to use low threshold voltage transistors for transistors **144** and **148**. However, leakage of current through transistors **144** and **148** will affect the robustness of this prior art design. Since lower threshold voltage transistors are more susceptible to leakage, they can not be employed without addressing their susceptibility. Leakage is undesirable as it may cause erroneous evaluations if too much charge is lost. In contrast, using high threshold voltage transistors results in an unacceptably long read delay as the increased threshold voltages increase response times.

[0006] Keeper circuits have been used to increase the robustness of the dynamic local bit line design. Keeper circuits are utilized to maintain the

precharged value on the dynamic local bit line **110** in cases where low threshold voltage transistors **144 148** may otherwise allow the improper discharge of the precharged value via leakage current. In order to maintain the prechared value on the local bit line, an upsized transistor **132** is utilized as part of the keeper circuitry **130**. However, this upsized keeper also results in a read delay that may be unacceptable for the next generation's high operating frequencies.

[0007] Thus, a register file design that is robust, while still being able to operate at high operating frequencies is desired.

BRIEF DESCRIPTION OF THE DRAWINGS

[0008] Embodiments of the present invention will be described referencing the accompanying drawings in which like references denote similar elements, and in which:

[0009] FIG. 1 (Prior Art) illustrates a read portion of a dynamic register file design.

[0010] FIG. 2 illustrates a dynamic register file organization with two level multiplexing, in accordance with one embodiment.

[0011] FIG. 3 illustrates a truth table for a decoder selected keeper function, in accordance with one embodiment.

[0012] FIGs. 4A and 4 B illustrate a gate level implementation of a decoder selected keeper function, in accordance with one embodiment.

[0013] FIG. 5 illustrates a transistor level implementation of a decoder selected keeper function, in accordance with one embodiment.

[0014] FIG. 6 illustrates a block diagram of a computer system including a register file with selectable keeper.

DETAILED DESCRIPTION OF THE EMBODIMENTS

[0015] In the following description, various aspects of the embodiments of the invention will be described. However, it will be apparent to those skilled in the art that other embodiments may be practiced with only some or all of these aspects. For purposes of explanation, specific numbers, materials and configurations are set forth in order to provide a thorough understanding of these embodiments. However, it will also be apparent to one skilled in the art that other embodiments may be practiced without the specific details. In other instances, well-known features are omitted or simplified in order not to obscure the description.

[0016] Keeper refers to a circuit added to a dynamic node to maintain that node at a predetermined voltage level. Typically, a keeper is added to a node that, in operation, will periodically be precharged high. The keeper supplies the charge necessary to compensate for the loss of charge due to various leakage paths, as well as loss of charge due to capacitive coupling of the node to other signal paths. A half-keeper is a circuit providing a switchable, direct, conductive pathway between the dynamic node and one voltage source, e.g., a positive voltage source, and therefore operable only to maintain the dynamic node at one level, e.g., a high level. A full-keeper is a circuit providing a switchable, direct, conductive pathway between the dynamic node and two voltage sources, e.g., a positive voltage and ground, and therefore operable to maintain the dynamic node at either a high or low level. A keeper-interrupt is a circuit providing a switchable, direct, conductive pathway between the dynamic node and a first voltage source, e.g., a positive voltage, and a switchable, indirect pathway

between the dynamic node and a second voltage source, e.g., ground. In a keeper-interrupt circuit, there is at least one switchable circuit element coupled between the dynamic node and keeper-interrupt pathway to the second voltage source.

[0017] The terms metal line, trace, wire, conductor, signal path and signaling medium are all related. The related terms listed above, are generally interchangeable, and appear in order from specific to general. In this field, metal lines are sometimes referred to as traces, wires, lines, interconnect or simply metal. Metal lines, generally aluminum (Al), copper (Cu) or an alloy of Al and Cu, are conductors that provide signal paths for coupling or interconnecting, electrical circuitry. Conductors other than metal are available in microelectronic devices. Materials such as doped polysilicon, doped single-crystal silicon (often referred to simply as diffusion, regardless of whether such doping is achieved by thermal diffusion or ion implantation), titanium (Ti), molybdenum (Mo), and refractory metal salicides are examples of other conductors.

[0018] FIG. 2 illustrates a dynamic register file organization including 3-stack dynamic gate with two level multiplexing, in accordance with one embodiment. The first level of multiplexing **290** comprises a number of two stack eight-way local bit lines **240**. The second level multiplexing **295** corresponds to a "higher-level" global bit line **210**.

[0019] In the embodiment illustrated, during the precharge portion of a clock cycle, clock signal **280** is utilized to facilitate precharging global bit line **210** to supply voltage, Vcc **207,** through transistor **282**. In addition, local bit lines **240** are

precharged to supply voltage, Vcc **207**, utilizing clock signal **280** driving transistor **284** to a voltage level lower than the supply voltage Vcc by value equal to the threshold voltage, Vth, of transistors **286**.

[0020] Global bit line **210** is coupled to supply voltage **205** through keeper device **215**. Keeper device is intended to "keep" the precharge value on the global bit during the evaluation phase if the global bit line does not evaluate to a different value than the precharge value. However, when keeper device **215** comprises a weak P-type MOS device, it may be unable to prevent global bit line **210** from undesirably discharging through the three stack dynamic gates. This undesirable discharge occurs when there was no evaluation of the local bit line stage **290** designed to result in the local bit line changing to a different value. For example, assume a logic "1" on the D0 **270** line and an enabled selected line **250** on select transistor **252** as this select line may be shared with other second level global bit line stages. Further assume that, due to coupling on read select lines **260** which drive read select transistors **262**, the voltage level on read select signal trace **260** rises above the transistor's threshold voltage. Under these conditions, current may discharge to ground through the three stack pulldown **252 262 272**. There may be a particular susceptibility to this if low threshold voltages transistors are used for the three stack pulldown **252 262 272.**

[0021] One solution is to utilize an upsized PMOS transistor on keeper **215**. However, usage of an upsized PMOS device as a keeper **215** may prevent the global bit line **210** from being able to properly evaluate. That is, during the evaluation phase for the register file bit lines, an upsized keeper may prevent the

timely discharge of current to ground when a data line has been selected. For example, in the embodiment illustrated in FIG. 2, if read select, RS0 **260**, and second level select, S0 **250**, are both enabled and D0 **270** is a logic "1", then the global bit line **210** is designed to discharge to lower potential, thus providing the proper value on output signal trace **203**. However, if an upsized keeper is utilized, there may not be sufficient time to fully discharge the global bit line **210** to the proper lower potential.

[0022] In the embodiment illustrated, the supply voltage **205** is intelligently decoupled from global bit line **210**. Referring again to the prior art implementation, recall that the value on the bit line itself is utilized to "keep" the value on the bit line (e.g. by controlling the keeper via gate voltage) utilizing feedback through the keeper device. In the embodiment illustrated, instead of using the feedback value to couple the supply voltage to the bit line via gate control signal **201**, the coupling is intelligently controlled. Thus, the global bit line **210** may be decoupled from the supply voltage **205** upon determination that one of the local bit lines **240** will evaluate. This may be performed, for example, by having a decoder selected keeper function control keeper device **215** via gate **201**. In this manner, an upsized PMOS device may be utilized for keeper device **215** while still enabling the global bit line **210** to timely evaluate.

[0023] FIG. 3 illustrates a truth table for a decoder selected keeper function, in accordance with one embodiment. Shown is the function for the decoupling of the global bit line based on the evaluation of one of the local bit lines. The keeper function, F **310**, is asserted, indicating that the decoupling should occur, as a

result of the local bit line being selected (S = 1) and the local bit line having evaluated (LBL=0). An overall function for the intelligent decoupling of the global bit line may be obtained utilizing the keeper functions, F **310**, for each of the local bit lines. Since the decoupling of the global bit line occurs when *any* of the local bit lines evaluate, the intelligent decoding may be the logical OR of each local bit line's function.

[0024] FIGs. 4A and 4B illustrate a gate level implementation of a decoder selected keeper function, in accordance with one embodiment. As illustrated in FIG 4A, a local bit line decoupling signal **405** may be generated corresponding to each local bit line. Each local bit line signal **460** and corresponding select signal **462** are utilized by local bit line decouple circuit **410** to generate a local bit line decoupling signal **405**. As illustrated in FIG. 4B, the local bit line decoupling signals **405** are then ORed to obtain a keeper select signal **401**. In this manner, the keeper turns off when the global bit line evaluates. Moreover, the decoder circuit advantageously computes the condition in parallel to the evaluation of the global bit line.

[0025] FIG. 5 illustrates a transistor level implementation of a decoder selected keeper function, in accordance with one embodiment. As previously discussed, the decoder selected keeper function provides intelligent decoupling of keeper signal from voltage source. The transistor level circuit of FIG. 5 implements the function, F **310**, of FIG 3. Thus, if any local bit line evaluates **530** and a corresponding select signal **540** is asserted, the pull down network **520** is shut

off. Under these conditions, a corresponding stage **550** of the pull up network **510** will be enabled, bringing output F **560** to a logic "1".

[0026] In this embodiment, a transistor level implementation may be utilized to reduce the area overhead of the keeper turn-off circuit in comparison to a gate level implementation. In addition, in such an embodiment, the design may utilize minimum sized transistors to further reduce the area of the keeper decoupling circuit and to reduce switching energy overhead associated with the keeper decoupling circuit.

[0027] FIG. 6 illustrates a block diagram of a computer system **600** including a register file with selectable keeper **602**. As shown, the computer system **600** includes a processor **610** and temporary memory **620**, such as SDRAM and DRAM, on high-speed bus **605**. Register file **602**, incorporated with the earlier described selectable keeper teachings, advantageously provides high speed, yet robust, access to memory for processor **610**. High-speed bus is connected through bus bridge **630** to input/output (I/O) bus **615**. I/O bus **615** connects permanent memory **640**, such as flash devices and fixed disk device, and I/O devices **650** to each other and bus bridge **630**.

[0028] Thus, a more robust design of the dynamic bit lines of high performance register file is disclosed. While the invention has been described in accordance with a number of embodiments, the invention should not be considered so limited. One skilled in the art will recognize that various other embodiments can be utilized to provide the advantages described herein.